HX8218-A
960CH TFT LCD Source Driver with Built-in TCON
Application Note

Preliminary Version 0.5

Jun. 2005

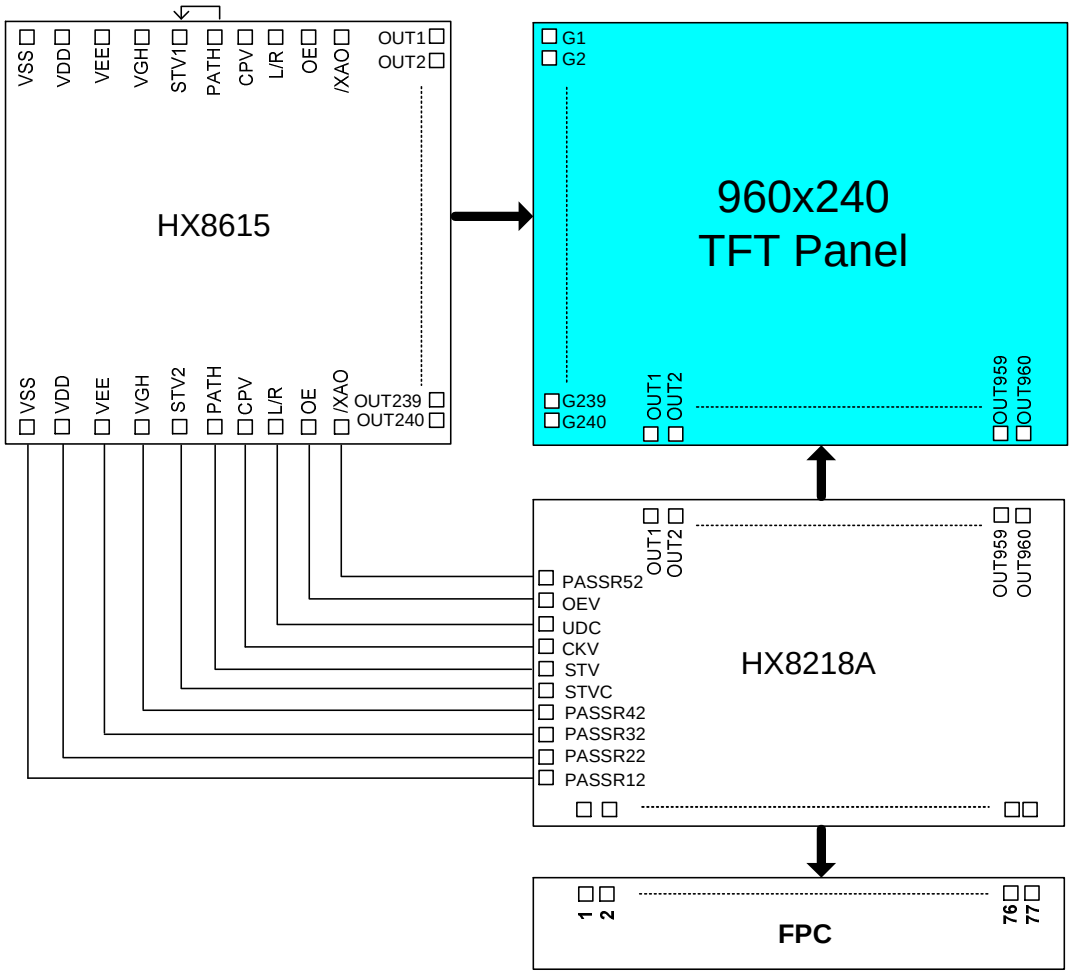
1. General Description

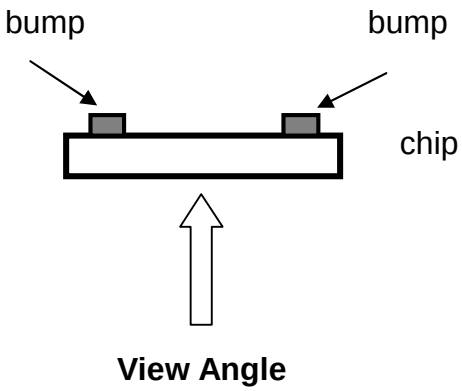
HX8218-A is a 960-channel output Source Driver with built-in TCON and DAC. The interface follows digital 8-bits serial/24-bits parallel RGB, or CCIR601/656 input signals and digital control timing signals. The DAC supports transferring digital RGB data to analog RGB data for the internal Source Driver. The TCON generates the 960x240 resolution timing to Source driver and Gate Driver.

The Source Driver implements 2 lines of sample and hold circuits. While sampling video signals, the previously sampled data can be output synchronously through driver output channels. And simultaneous or sequential sampling can be chosen for matching the pixel array type.

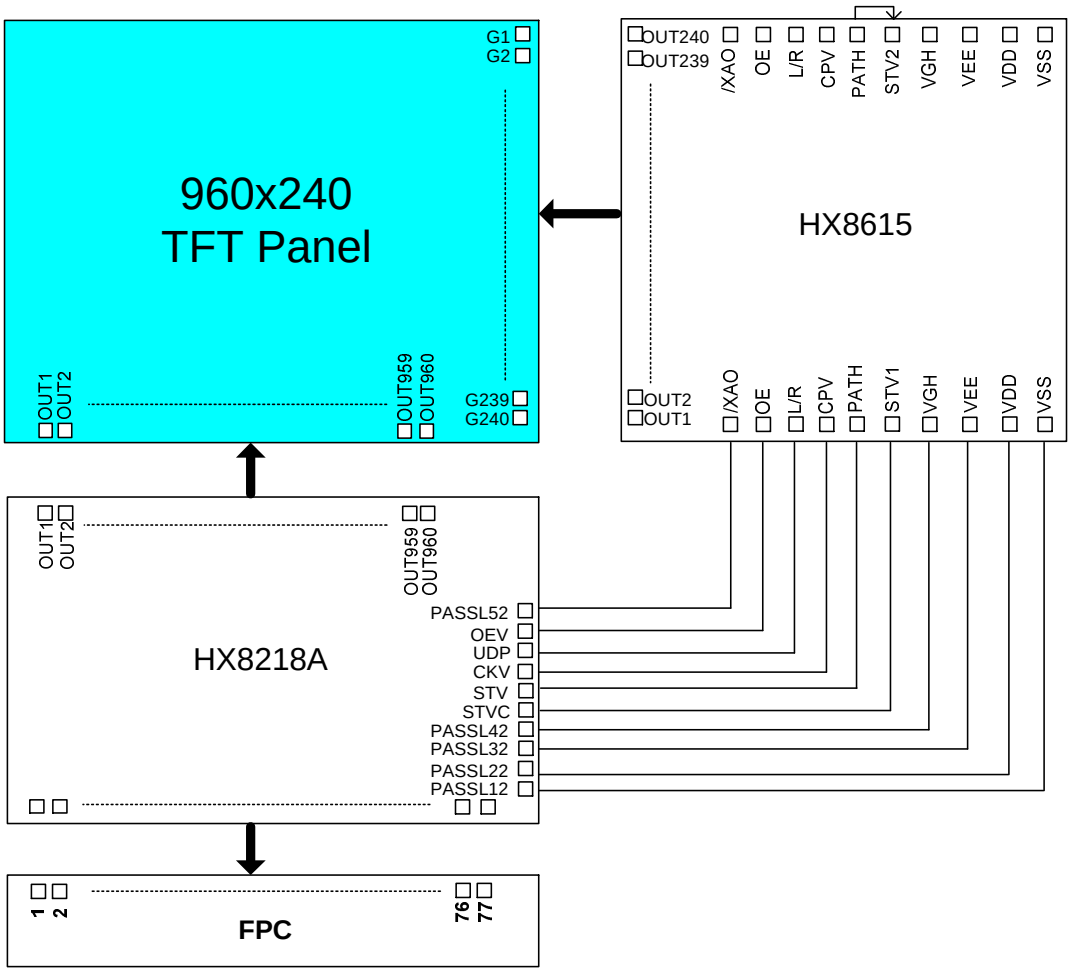
The timing controller provides horizontal and vertical control timing to source and gate drivers. With built-in DAC and operational amplifiers, the gamma correction can be performed and digital data is converted to analog signal and sends to source driver.

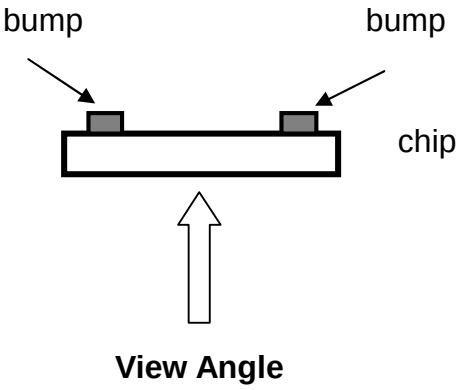
2. On Panel Connection (L)



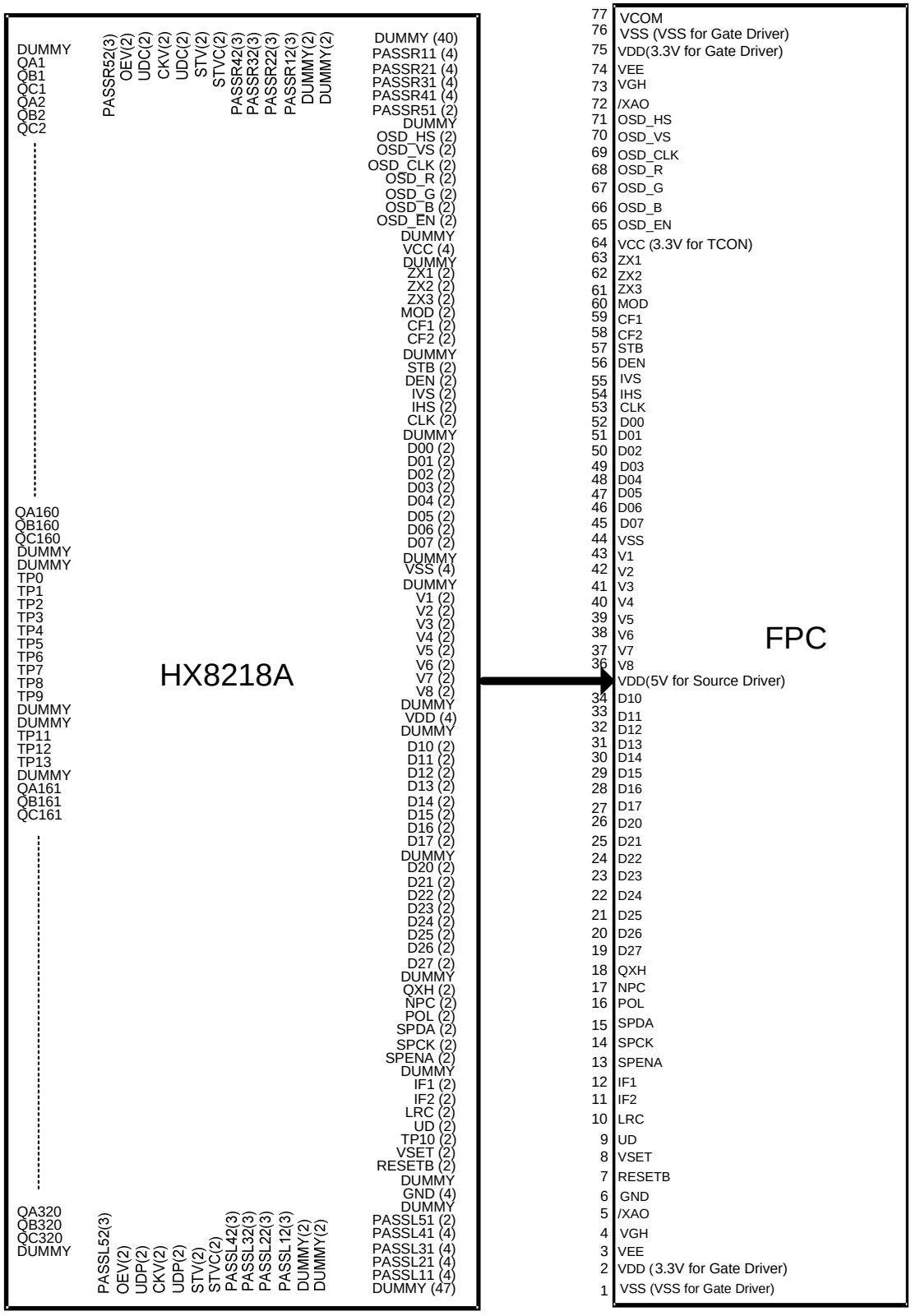


3. On Panel Connection (R)





4. FPC


DUMMY
QA1
QB1
QC1
QA2
QB2
QC2
QA160
QB160
QC160
DUMMY
DUMMY
TP0
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
DUMMY
DUMMY
TP11
TP12
TP13
DUMMY
QA161
QB161
QC161
QA320
QB320
QC320
DUMMY
PASSR52(3)
OEV(2)
UDC(2)
CKV(2)
UDC(2)
STV(2)
STVC(2)
PASSR42(3)
PASSR32(3)
PASSR22(3)
PASSR12(3)
DUMMY(2)
DUMMY(2)
PASSL52(3)
OEV(2)
UDP(2)
CKV(2)
UDP(2)
STV(2)
STVC(2)
PASSL42(3)
PASSL32(3)
PASSL22(3)
PASSL12(3)
DUMMY(2)
DUMMY(2)
HX8218A
DUMMY (40)
PASSR11 (4)
PASSR21 (4)
PASSR31 (4)
PASSR41 (4)
PASSR51 (2)
DUMMY
OSD_HS (2)
OSD_VS (2)
OSD_CLK (2)
OSD_R (2)
OSD_G (2)
OSD_B (2)
OSD_EN (2)
DUMMY
VCC (4)
DUMMY
ZX1 (2)
ZX2 (2)
ZX3 (2)
MOD (2)
CF1 (2)
CF2 (2)
DUMMY
STB (2)
DEN (2)
IVS (2)
IHS (2)
CLK (2)
DUMMY
D00 (2)
D01 (2)
D02 (2)
D03 (2)
D04 (2)
D05 (2)
D06 (2)
D07 (2)
DUMMY
VSS (4)
DUMMY
V1 (2)
V2 (2)
V3 (2)
V4 (2)
V5 (2)
V6 (2)
V7 (2)
V8 (2)
DUMMY
VDD (4)
DUMMY
D10 (2)
D11 (2)
D12 (2)
D13 (2)
D14 (2)
D15 (2)
D16 (2)
D17 (2)
DUMMY
D20 (2)
D21 (2)
D22 (2)
D23 (2)
D24 (2)
D25 (2)
D26 (2)
D27 (2)
DUMMY
QXH (2)
NPC (2)
POL (2)
SPDA (2)
SPCK (2)
SPENA (2)
DUMMY
IF1 (2)
IF2 (2)
LRC (2)
UD (2)
TP10 (2)
VSET (2)
RESETB (2)
DUMMY
GND (4)
DUMMY
PASSL51 (2)
PASSL41 (4)
PASSL31 (4)
PASSL21 (4)
PASSL11 (4)
DUMMY (47)
77 VCOM
76 VSS (VSS for Gate Driver)
75 VDD(3.3V for Gate Driver)
74 VEE
73 VGH
72 /XAO
71 OSD_HS
70 OSD_VS
69 OSD_CLK
68 OSD_R
67 OSD_G
66 OSD_B
65 OSD_EN
64 VCC (3.3V for TCON)
63 ZX1
62 ZX2
61 ZX3
60 MOD
59 CF1
58 CF2
57 STB
56 DEN
55 IVS
54 IHS
53 CLK
52 D00
51 D01
50 D02
49 D03
48 D04
47 D05
46 D06
45 D07
44 VSS
43 V1
42 V2
41 V3
40 V4
39 V5
38 V6
37 V7
36 V8
35 VDD(5V for Source Driver)
34 D10
33 D11
32 D12
31 D13
30 D14
29 D15
28 D16
27 D17
26 D20
25 D21
24 D22
23 D23
22 D24
21 D25
20 D26
19 D27
18 QXH
17 NPC
16 POL
15 SPDA
14 SPCK
13 SPENA
12 IF1
11 IF2
10 LRC
9 UD
8 VSET
7 RESETB
6 GND
5 /XAO
4 VGH
3 VEE
2 VDD (3.3V for Gate Driver)
1 VSS (VSS for Gate Driver)
FPC

5. Pin in FPC

5.1 Input Data Mode in FPC

	D00 ~ D07	D10 ~ D17	D20 ~ D27
Serial RGB	V	X	X
Parallel RGB	V	V	V
CCIR 656	V	X	X
CCIR 601	V	X	X

5.2 Input Data Format Setting

IF2	IF1	Input data format
L	L	Serial RGB (default)
L	H	Parallel RGB
H	L	CCIR601
H	H	CCIR656

5.3 Description in FPC

5.3.1 OSD : If you don't want to use OSD, you just set the OSD_EN to low and others(OSD_HS, OSD_VS, OSD_CLK, OSD_R, OSD_G, OSD_B) are floating.

5.3.2 SPI : If you don't want to use SPI, you just set the SPENA to high and others(SPDA, SPCK) are floating.

5.3.3 Gamma Voltage : Set VSET to low to use the default voltage and others(V1 ~ V8) are floating.

5.3.4 Color Filter : When MOD="L", delta type.

When MOD="H", stripe type and others(CF1, CF2) are floating.

5.3.5 Input data sequence and color filter type

- CF1 defines the input data sequence in serial digital RGB mode as following tables.

1. CF1="L"

Scan direction	UD	Low	Low	High	High
Shift direction	LRC	High	Low	High	Low
Data sequence	Odd line	RGB	BGR	BRG	GRB
	Even line	BRG	GRB	RGB	BGR

2. CF1="H"

Scan direction	UD	Low	Low	High	High
Shift direction	LRC	High	Low	High	Low
Data sequence	Odd line	RGB	BGR	GBR	RBG
	Even line	GBR	RBG	RGB	BGR

- For the color filter type, set MOD="H" for stripe type and the CF1&CF2 definition will have no meaning. Set MOD="L" for delta color filter and CF2 defines which kind of delta type color filter is used.

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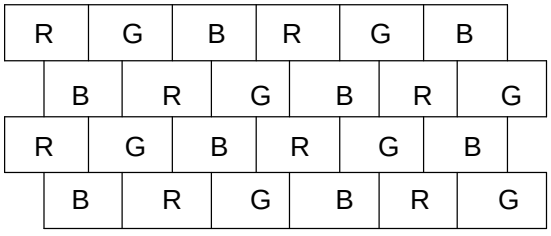
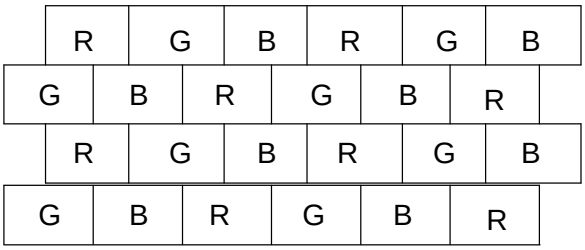
1. CF2="L", delta type 1



2. CF2="H", delta type 2:



5.3.6 Zoom Mode : The zoom in/out function is only supported in CCIR601/656 input mode in Strip type.

5.3.7 **Hardware Global Reset : Low active. Normally pull high.**

5.3.8 VCOM : VCOM and POL are inphase.

6. Power ON/OFF sequence

To prevent the device from damage due to latch-up, the power ON/OFF sequence shown below must be followed.

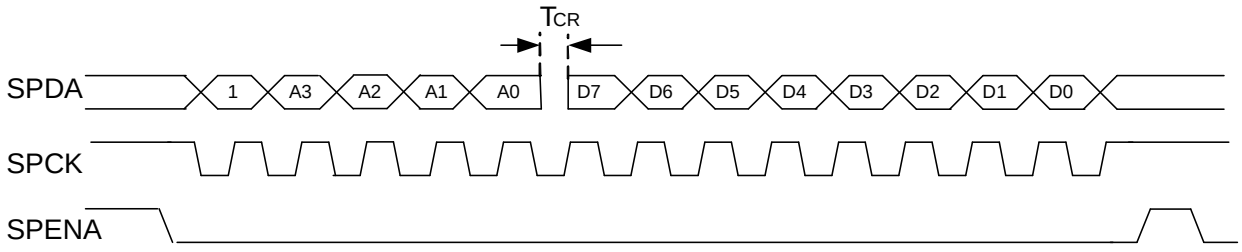
Power ON: VCC, GND → VDD, VSS → V1~V8

Power OFF: V1~V8 → VDD, VSS → VCC, GND

7. SPI

7.1 Description

- **SPI "read" timing**

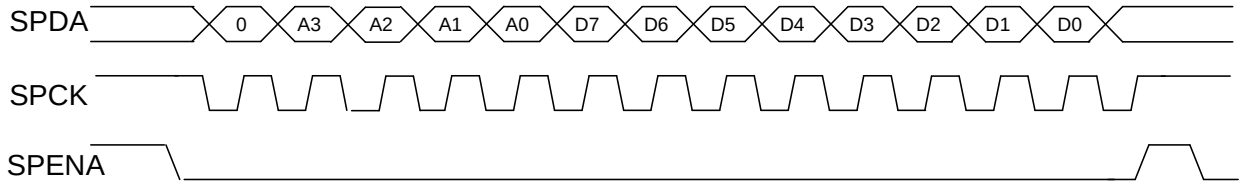


(1) Make a clock (2 MHZ) for SPCK.

(2) Set SPENA low to let the SPI valid.

(3) Send "1" in the MSB to show reading the SPI and the address 4-bits (A3 : MSB, A0 : LSB) in the rising edge of the SPCK then wait a half of the SPCK to read the data(D7 : MSB, D0 : LSB) in the falling edge of the SPCK.

- **SPI "write" timing**

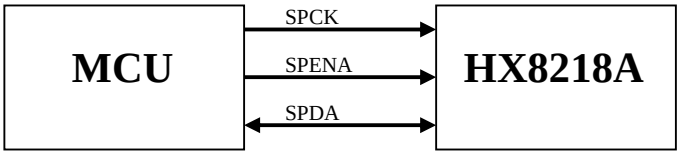


(1) Make a clock (2 MHZ) for SPCK.

(2) Set SPENA low to let the SPI valid.

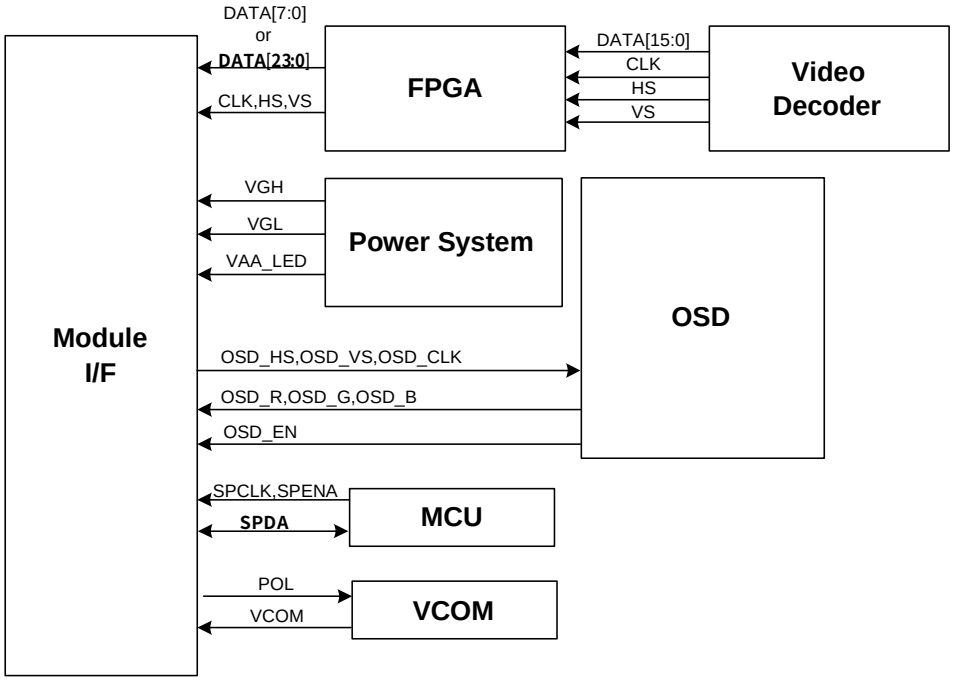
(3) Send “0” in the MSB to show writing the SPI and the address 4-bits (A3 : MSB, A0 : LSB) in the rising edge of the SPCK then read the data(D7 : MSB, D0 : LSB) in the rising edge of the SPCK.

7.2 Follow

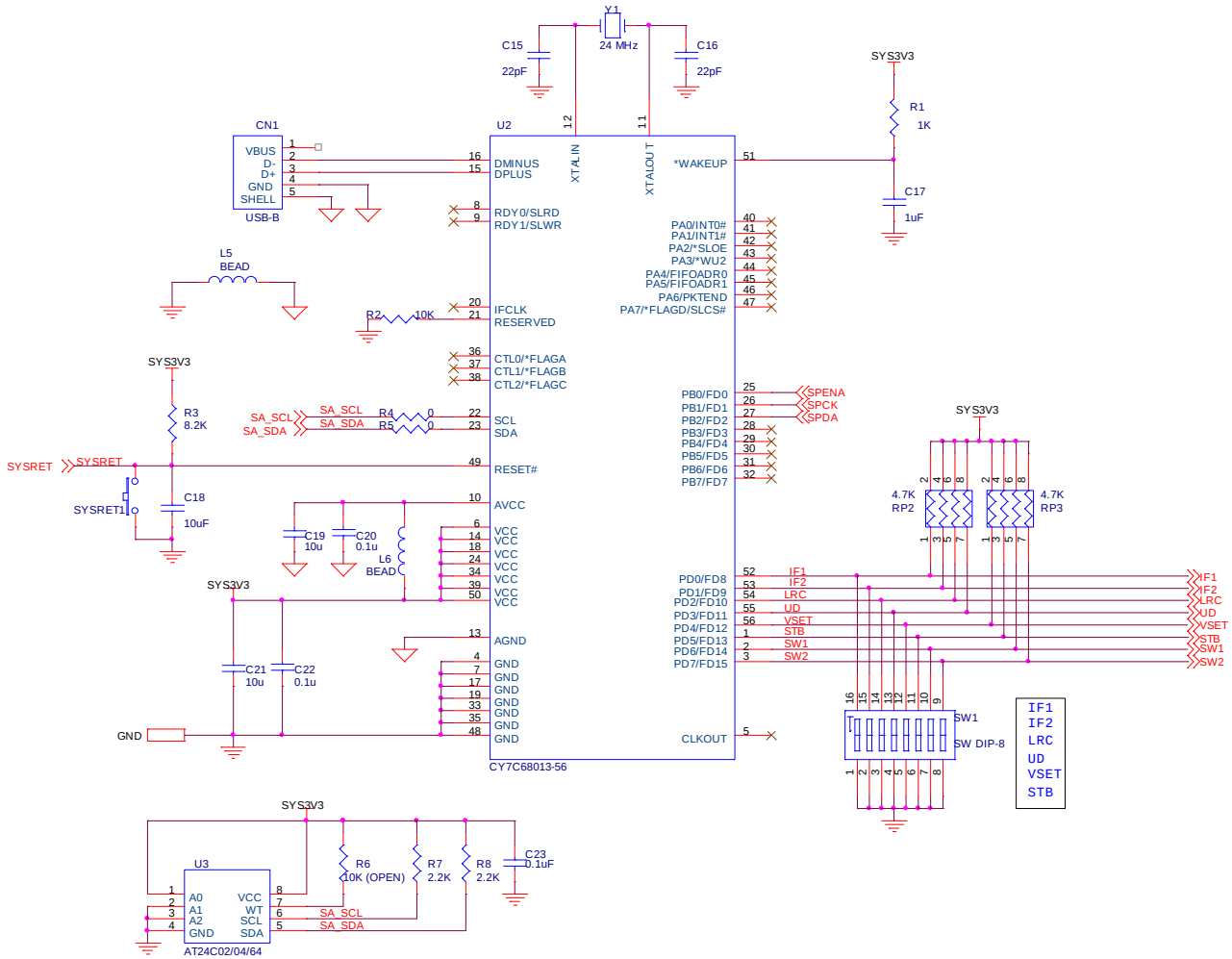


8. Reference Circuit

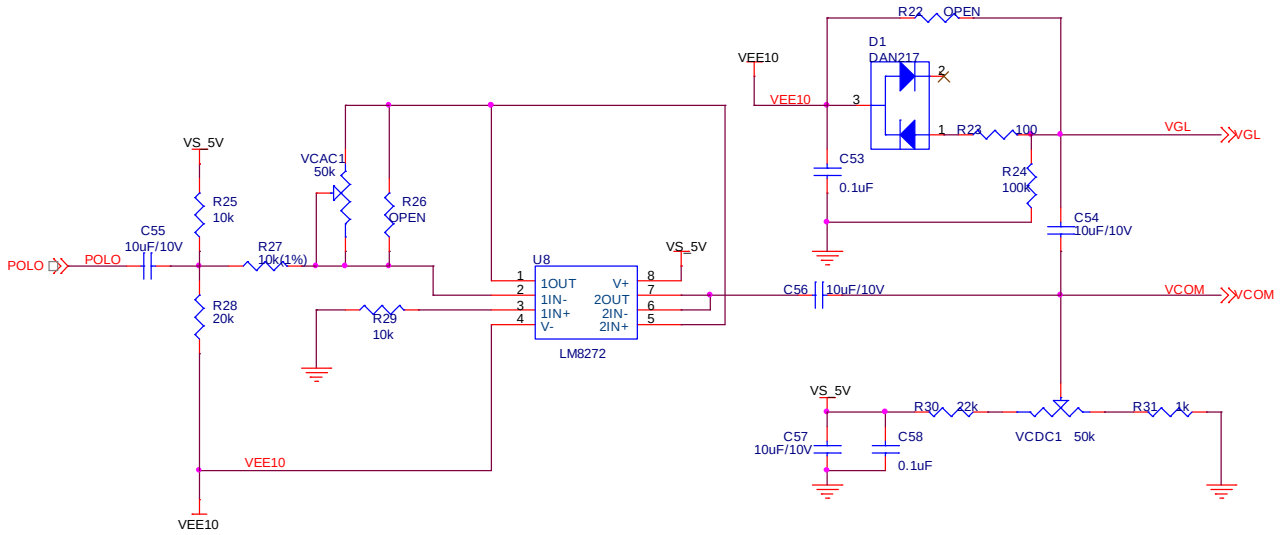
8.1 System Block



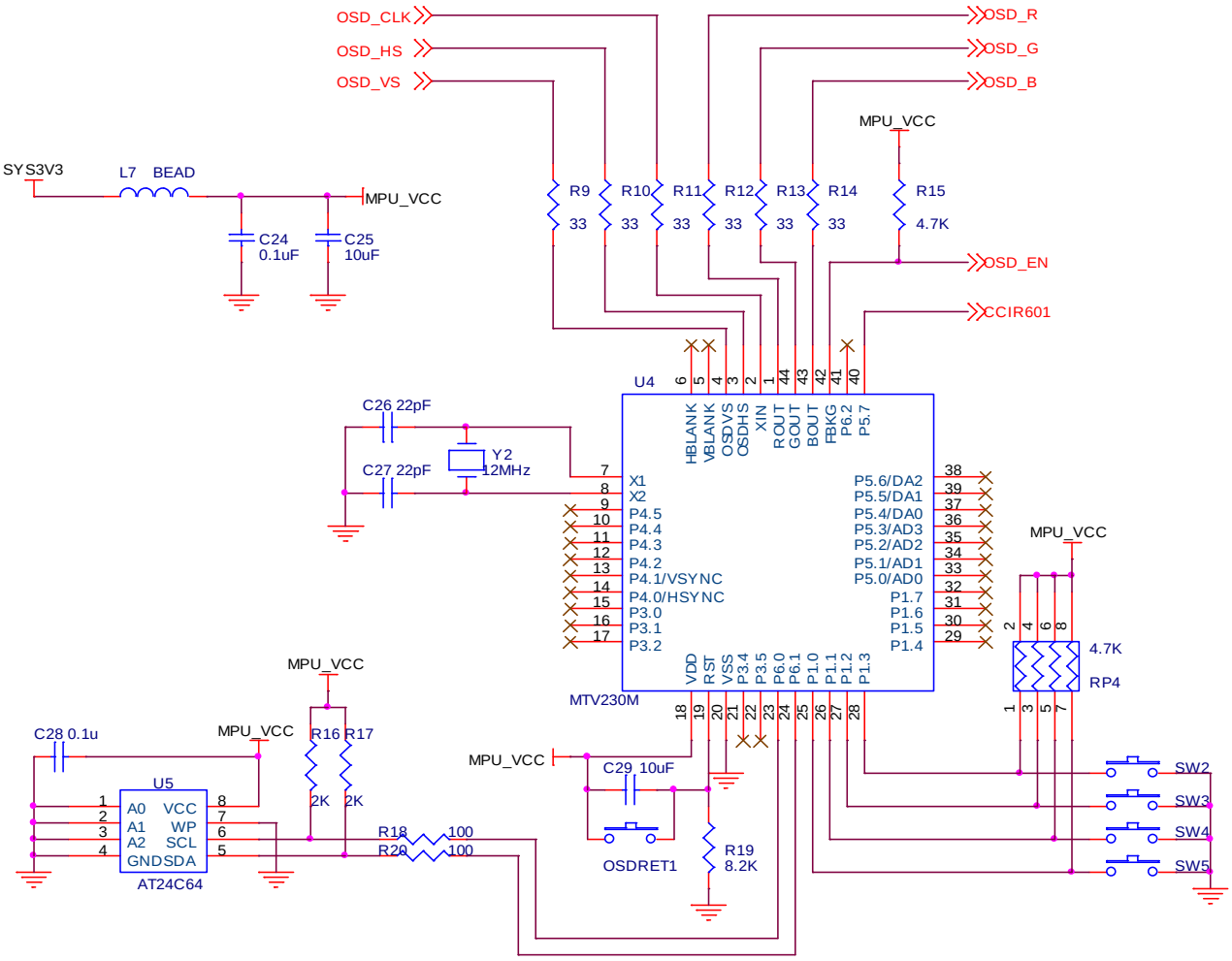
8.2 MCU



8.3 VCOM



8.4 OSD


OSD_CLK
OSD_HS
OSD_VS
OSD_R
OSD_G
OSD_B
MPU_VCC
SYS3V3
L7 BEAD
MPU_VCC
C24 0.1uF
C25 10uF
R9 33
R10 33
R11 33
R12 33
R13 33
R14 33
R15 4.7K
OSD_EN
CCIR601
U4
HBLANK
VBLANK
OSDVS
OSDHS
XIN
ROUT
GOUT
BOUT
FBKG
P6.2
P5.7
C26 22pF
C27 22pF
Y2 12MHz
X1
X2
P4.5
P4.4
P4.3
P4.2
P4.1/VSYNC
P4.0/HSYNC
P3.0
P3.1
P3.2
P5.6/DA2
P5.5/DA1
P5.4/DA0
P5.3/AD3
P5.2/AD2
P5.1/AD1
P5.0/AD0
P1.7
P1.6
P1.5
P1.4
MPU_VCC
4.7K
RP4
MTV230M
VDD
RST
VSS
P3.4
P3.5
P6.0
P6.1
P1.0
P1.1
P1.2
P1.3
MPU_VCC
C28 0.1u
MPU_VCC
R16 R17
2K 2K
U5
A0 VCC
A1 WP
A2 SCL
GND SDA
AT24C64
MPU_VCC
C29 10uF
OSDRET1
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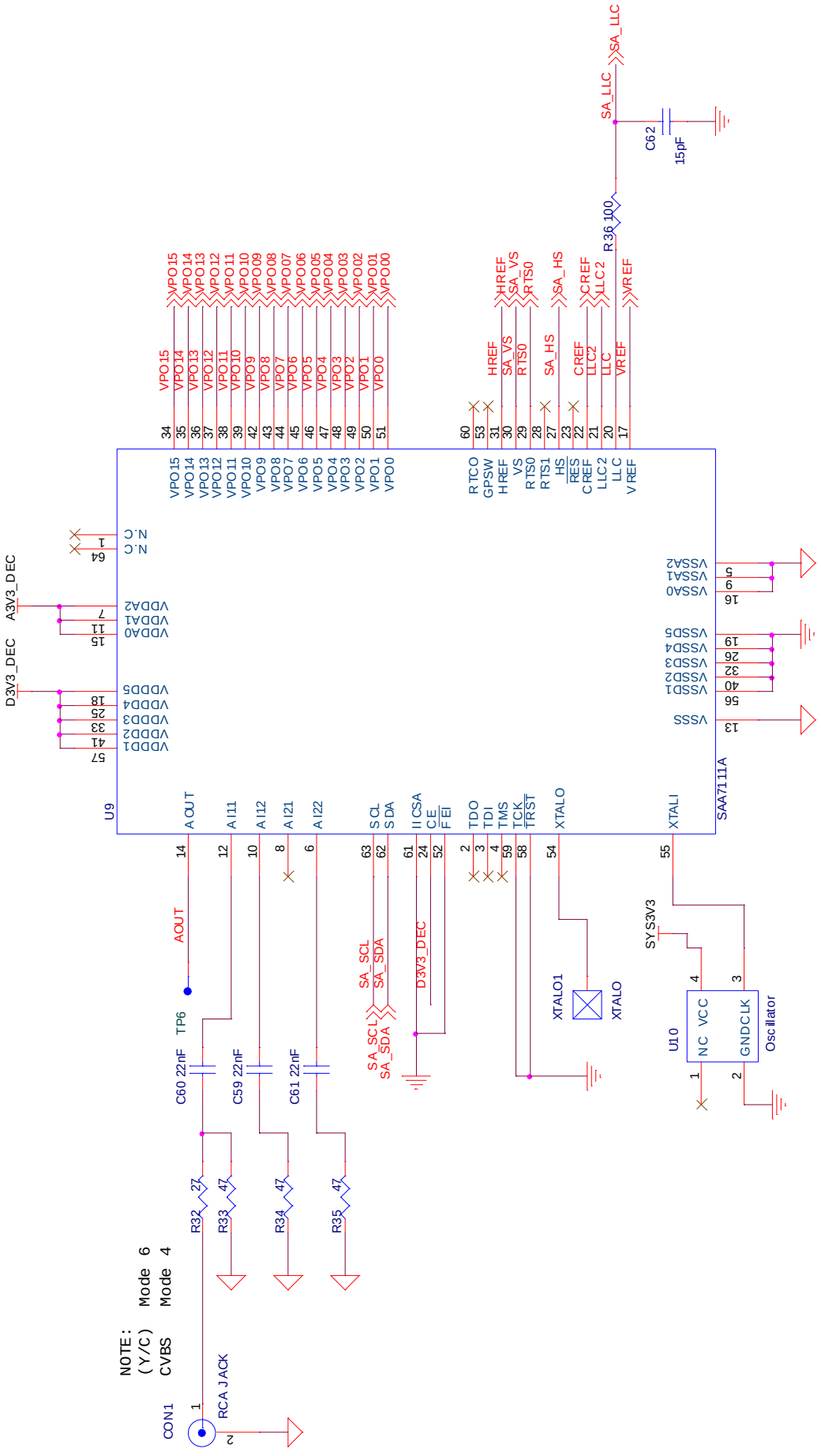
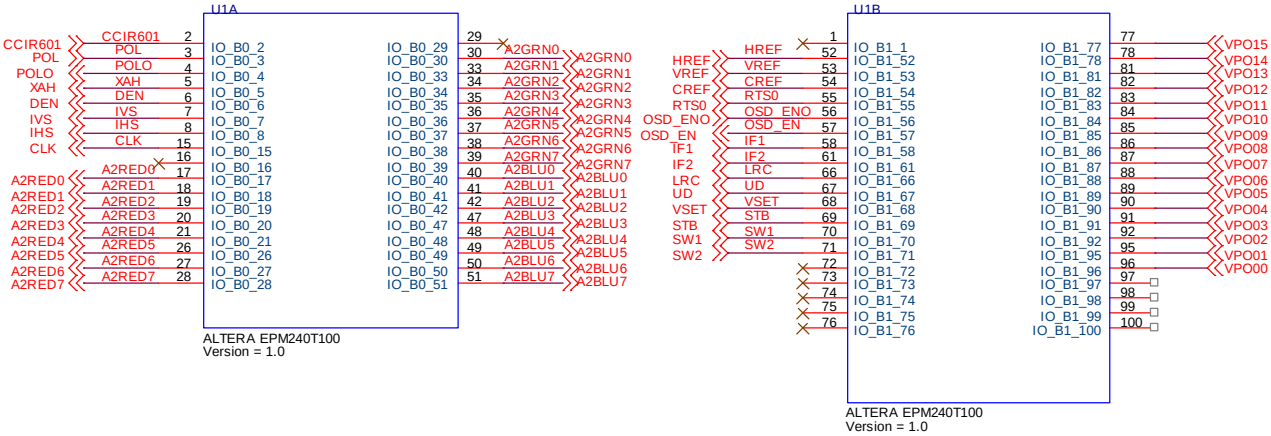
R20 100
R19 8.2K
SW2
SW3
SW4
SW5

8.5 Video Decoder



8.6 FPGA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CCIR601
POL
POLO
XAH
DEN
IVS
IHS
CLK
A2RED0
A2RED1
A2RED2
A2RED3
A2RED4
A2RED5
A2RED6
A2RED7
IO_B0_2
IO_B0_3
IO_B0_4
IO_B0_5
IO_B0_6
IO_B0_7
IO_B0_8
IO_B0_15
IO_B0_16
IO_B0_17
IO_B0_18
IO_B0_19
IO_B0_20
IO_B0_21
IO_B0_26
IO_B0_27
IO_B0_28
IO_B0_29
IO_B0_30
IO_B0_33
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IO_B0_39
IO_B0_40
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IO_B0_48
IO_B0_49
IO_B0_50
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A2GRN5
A2GRN6
A2GRN7
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A2BLU3
A2BLU4
A2BLU5
A2BLU6
A2BLU7
ALTERA EPM240T100
Version = 1.0
U1B
HREF
VREF
CREF
RTS0
OSD_ENO
OSD_EN
IF1
IF2
LRC
UD
VSET
STB
SW1
SW2
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IO_B1_52
IO_B1_53
IO_B1_54
IO_B1_55
IO_B1_56
IO_B1_57
IO_B1_58
IO_B1_61
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IO_B1_68
IO_B1_69
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VPO12
VPO11
VPO10
VPO09
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VPO07
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VPO05
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VPO01
VPO00
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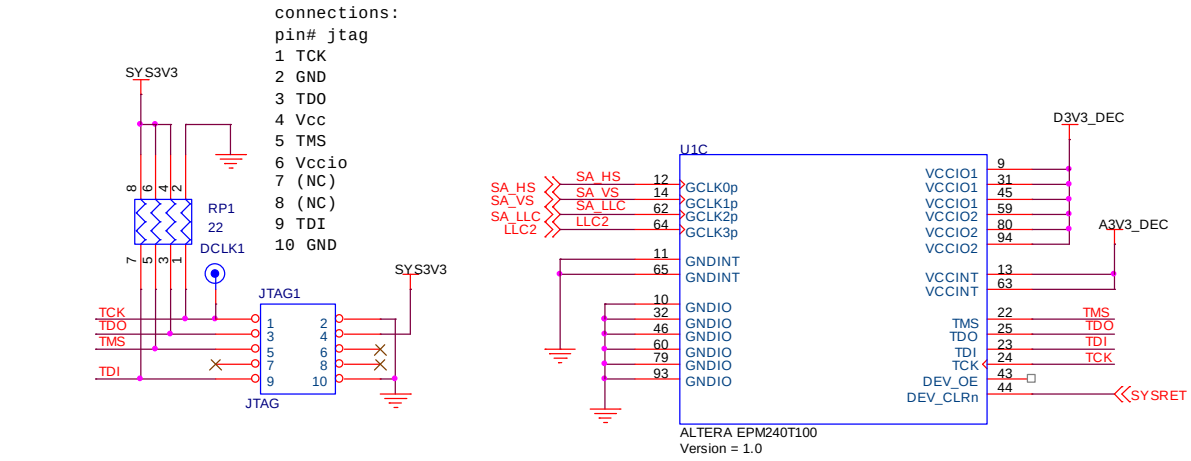
Version = 1.0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1 TCK
2 GND
3 TDO
4 Vcc
5 TMS
6 Vccio
7 (NC)
8 (NC)
9 TDI
10 GND
SYS3V3
RP1
22
DCLK1
JTAG1
JTAG
TCK
TDO
TMS
TDI
U1C
SA_HS
SA_VS
SA_LLC
LLC2
GCLK0p
GCLK1p
GCLK2p
GCLK3p
GNDINT
GNDIO
VCCIO1
VCCIO2
VCCINT
TMS
TDO
TDI
TCK
DEV_OE
DEV_CLRn
D3V3_DEC
A3V3_DEC
SYSRET
ALTERA EPM240T100
Version = 1.0